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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attention: Examiner R. Pompey
Art Unit: 2812

Re: M. YOSHIDA, et al. – Application No.: 09/416,959
Our Ref. No.: 501.35437CV2

SUBMISSION OF DOCUMENT

Sir:

Applicants hereby submit the attached "Request for Reconsideration" (6 pgs) in the above-identified application.

CERTIFICATE OF TRANSMISSION:

I hereby certify that the attached "Request for Reconsideration" (6 pgs), is being formally filed via the USPTO Central Fax No. 703-872-9306 on **April 15, 2004**.

Deborah L. Therrien

501.35437CV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	M. YOSHIDA et al.
Application No.:	09/416,959
Filed:	October 13, 1999
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME
Art Unit:	2812
Examiner:	R. Pompey

REQUEST FOR RECONSIDERATION
AND
STATEMENT OF SUMMARY OF INTERVIEW

April 15, 2004

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Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

This Request for Reconsideration is in response to the response to the Final Office Action dated January 15, 2004.

Prior to the filing of this Request for Reconsideration, a personal interview was conducted with Examiner Pompey on April 13, 2004. Appreciation is expressed to Examiner Pompey for his courtesy and helpfulness at this interview. The following remarks provide a statement of discussions conducted during the interview.

The first issue discussed at the interview was the 35 U.S.C. § 112, second paragraph, rejection of claims 50 and 51 as set forth in paragraph 5 of the Office

Action. Based upon the discussion and agreement at the interview, reconsideration and removal of this rejection is respectfully requested.

More specifically, the 35 U.S.C. § 112, first paragraph, rejection stated that claims 50 and 51 failed to comply with the enablement requirement. In particular, it was stated that there was no enablement for first silicide layers formed between surfaces of the first semiconductor regions and the plurality of first conductor plugs.

As discussed during the interview, the first conductor plugs defined in claims 50 and 51 can be read on the plugs 23 shown, for example, in Fig. 9 of the specification. The claimed first semiconductor regions can be read on the semiconductor regions such as indicated by numeral 11 (e.g. the source and drain regions of the memory cell) as discussed on page 11, lines 19 et seq. of the specification. With regard to this, it is noted that page 15, line 4 et seq. of the specification states, with regard to Fig. 9, that:

> "At this time, in order to reduce the contact resistance between the plugs 23 and the substrate, a Ti silicide ($TiSi_2$) film may be formed below the contact holes 17 to 22."

Noting that the regions 11 are provided in the substrate at the bottom of the contact holes in which the plugs 23 are formed, it was agreed during the interview that this provided support for the language of claims 50 and 51. Therefore, reconsideration and removal of the 35 U.S.C. § 112, first paragraph, rejection of claims 50 and 51 as not complying with the enablement requirement, as agreed during the interview, it respectfully requested.

Reconsideration and removal of the rejection of claims 42 and 50 over the combination of Wu (USP 4859619) in view of Ho (USP 4954214) and Tseng (USP

6090700) is also respectfully requested. During the interview, it was pointed out that the Wu reference differed from the claimed invention set forth in the independent claims 42 and 47 in at least two ways. In the first place, it was noted, and agreed by Examiner Pompey, that Wu forms a metalization 81 in one step to fill the holes 79 while simultaneously providing a metalization over the insulating film. As recognized by Examiner Pompey, this differs from the arrangement used in the present invention, as illustrated by Figs. 9 and 10, of first forming conductor plugs such as 23 in Fig. 9 followed by forming first conductive strips over one of the first conductor plugs in a separate manufacturing step from the first conductor plugs. As discussed during the interview, the problem with this difference between the single step metalization 81 of Wu and the claimed arrangement using conductor plugs and a first conductive layer formed in separate manufacturing steps is that the one step process leaves an indent in the upper surface of the metalization, as clearly shown in the drawings of Wu (e.g. see Fig. 7).

The second shortcoming of the primary reference to Wu in meeting the limitations of independent claims 42 and 47 is Wu's failure to line up the second openings (for the second conductor plugs) with the upper surfaces of the first conductor plugs, as set forth in both claims 42 and 47. Instead, as clearly shown in Fig. 7 of Wu, the second holes identified by the numeral 85 are offset from the upper surfaces of the portion of the metalization 81 in the first conductor holes 79. It would appear that one reason for this offset would be the dimples referred to above in the metalizations 81 caused by the one step process of formation.

In the Office Action, reference is made to the Tseng and Ho patents to attempt to overcome these recognized shortcomings of the primary reference to Wu.

However, as discussed during the interview, the combination of Tseng and Ho with Wu would require complete modification of Wu which none of the references suggest. In particular, as discussed during the interview, the Wu reference is specifically directed to an EPROM fabrication process (as set forth in the title, abstract, the explanation in the "Technical Filed", the summary of the invention and all of the claims). As such, an essential element in the Wu reference to form such an EPROM is a dual-gate structure such as shown in Fig. 7. More specifically, this dual gate structure requires a second gate 73 located over a first gate 69. As is clear from Fig. 7, this changes the level of the dual gate transistors relative to the single gate transistors formed in the device.

The references to Tseng and Ho, on the other hand, are both directed to flattening techniques for transistors (not memory arrays and not EPROMs with dual gates). As such, to combine Tseng and Ho with Wu would require the complete modification of Wu to not use the second gate such as 73 since this second gate prevents the use of flattening techniques such as used in Tseng and Ho. Of course, eliminating the second gate would eliminate the use of the Wu reference for fabricating EPROMs, which is the whole purpose of Wu. As noted during the interview, this falls within the area discussed in MPEP 2143.01 under the heading "The proposed modification cannot render the prior art unsatisfactory for its intended purpose." In referring to the case of *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984), this section of the MPEP states:

> "If proposed modifications would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

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In reviewing this portion of the MPEP, Examiner Pompey agreed during the interview that the proposed modification set forth in the Office Action would, indeed, render the Wu reference unsatisfactory for its intended purpose of fabricating EPROMs. Accordingly, as stated in the Interview Summary:

> "Mr. Montone pointed out that the primary reference used in the latest action used floating gate and non floating structures and therefore caused unevenness in the interlayer insulator. This unevenness would create dimples in the formation of contact plugs. Also, this unevenness would lead to improper combination with secondary references used, because they use non floating gate structures and planarize the interlayer insulator. The Examiner agrees that upon first glance that the primary (Wu) reference is overcome by this argument, but that further consideration of the Wu and further search is necessary in view of this new argument."

Accordingly, for the reasons discussed during the interview and set forth above, it is respectfully submitted that the combination of Wu with Tseng and Ho set forth in the Office Action is improper under the provisions of MPEP 2143.01, and, as such, reconsideration and removal of this rejection is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135

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(Docket No. 501.35437CV2), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

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